

# Claims

[c1] Having thus described our invention in detail, what we claim as new and desire to secure by the Letters PATENT is:

1. A method for fabricating a precision polysilicon resistor comprising:

providing a structure that includes at least one polysilicon resistor device region and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer;

selectively performing an ion implant and an activation anneal in the at least one other type of device region;

forming a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region; and

providing a predetermined resistance value to said polysilicon layer in said at least one polysilicon resistor device region.

[c2] 2. The method of Claim 1 wherein said at least one polysilicon device region comprises a semiconductor substrate, an optional first dielectric located on the substrate, said polysilicon layer located on the substrate or

the optional first dielectric and a second dielectric layer located on the polysilicon layer.

- [c3] 3. The method of Claim 1 wherein the other device regions comprise bipolar transistor devices, CMOS devices or combinations thereof.
- [c4] 4. The method of Claim 1 further comprising forming a patterned photoresist atop the at least one polysilicon resistor device region to protect the region during said selective ion implant.
- [c5] 5. The method of Claim 1 wherein said protective dielectric layer is a nitride.
- [c6] 6. The method of Claim 1 wherein said step of providing a predetermined resistance value to said polysilicon layer comprises ion implantation into the polysilicon layer.
- [c7] 7. The method of Claim 6 wherein said ion implantation comprises p or n-type dopants.
- [c8] 8. The method of Claim 7 wherein said ion implantation provides said polysilicon layer with a dopant concentration of from about  $1 \times 10^{14}$  to about  $1 \times 10^{21}$  atom/cm<sup>3</sup>.
- [c9] 9. The method of Claim 6 further comprising an annealing step after said ion implantation.

- [c10] 10. The method of Claim 9 wherein said annealing step is performed in an inert gas ambient that may optionally be mixed with less than about 10% oxygen.
- [c11] 11. The method of Claim 1 further comprising exposing end portions of said polysilicon layer after said step of providing a predetermined resistance value to said polysilicon layer.
- [c12] 12. The method of Claim 11 further comprising providing silicide contacts on the exposed polysilicon layer.
- [c13] 13. The method of Claim 12 wherein said silicide contacts are formed using a silicidation process.
- [c14] 14. The method of Claim 13 wherein said silicidation process comprises depositing a conductive metal and annealing to cause reaction of the conductive metal with the underlying polysilicon layer thereby forming said silicide contacts.
- [c15] 15. The method of Claim 14 wherein said conductive metal is selected from the group consisting of Co, Ni, Ti, W and alloys thereof.
- [c16] 16. The method of Claim 15 wherein said conductive metal is Co or Ti.
- [c17] 17. A process for fabricating a precision polysilicon re-

sistor comprising:

performing a rapid thermal anneal for an emitter/FET activation process on a wafer or chip having a partially formed polysilicon resistor having a polysilicon layer; depositing a protective layer over the polysilicon layer to protect the polysilicon layer against subsequent silicide processing; ion implanting a dopant into the polysilicon layer through the protective layer; and performing silicide processing to form the precision polysilicon resistor.

- [c18] 18. The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal to activate the resistor polysilicon ion implant dopant.
- [c19] 19. The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal.
- [c20] 20. The method of Claim 17 wherein said protective layer comprises a nitride.